REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes made to Table 1, updated paragraph 4.4.1f, and editorial changes throughout. ksr	03-02-21	Raymond Monnin
B	Added t_R and t_F to section 1.4, and updated boilerplate paragraphs. ksr	04-03-12	Raymond Monnin
C	Added devices 05 - 08, Update to 1.3, made changes to I_{IL} and I_{OZ} in Table I, made change to paragraph 4.2.2 and 4.4.1f, and updated boilerplate paragraphs. ksr	04-08-27	Raymond Monnin

REV																				
SHEET																				
REV	C	C	C	C	C	C														
SHEET	15	16	17	18	19	20														

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
01 - 07 - 30

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990

http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY, 32,000 GATES, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-01508**

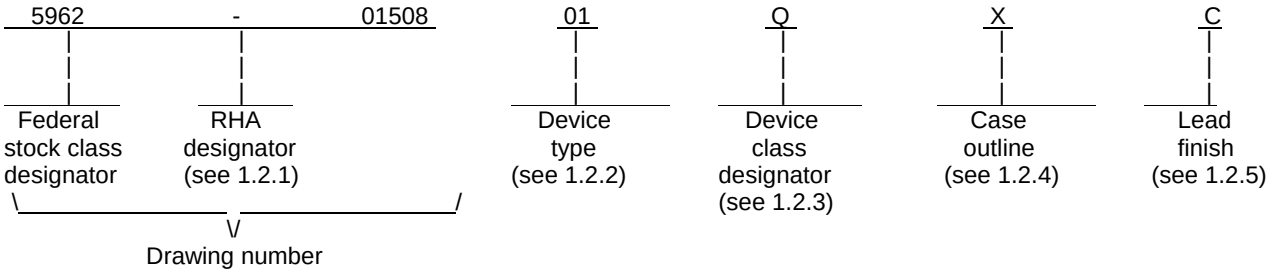
SHEET 1 OF 20

DSCC FORM 2233
APR 97

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	
01	RT54SX32S	32,000 gate field programmable gate array	
02	RT54SX32S-1	32,000 gate field programmable gate array	1/
03	RT54SX32S	32,000 gate field programmable gate array	2/
04	RT54SX32S-1	32,000 gate field programmable gate array	1/ 3/
05	RTSX32SU	32,000 gate field programmable gate array	
06	RTSX32SU-1	32,000 gate field programmable gate array	1/
07	RTSX32SU	32,000 gate field programmable gate array	4/
08	RTSX32SU-1	32,000 gate field programmable gate array	1/ 5/

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	256	Ceramic Quad Flat Pack
Y	See figure 1	208	Ceramic Quad Flat Pack

1/ Timing performance of the RT54SX32S-1 and RTSX32SU-1 devices shall be approximately 15% faster than the RT54SX32S and RTSX32SU devices (End users may select the appropriate device speed grade through timing calculations based on timing simulation of specific designs with manufacturer's Designer software. (see 6.7 herein)
2/ Device type 03 is device type 01 with additional testing (see 4.2.2 e)
3/ Device type 04 is device type 02 with additional testing (see 4.2.2 e)
4/ Device type 07 is device type 05 with additional testing (see 4.2.2 e)
5/ Device type 08 is device type 06 with additional testing (see 4.2.2 e)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings (for 2.5V/3.3V/5.0V operating conditions). 4/

DC supply voltage range (V_{CCI}) ..... -0.3 to +6.0 V dc
DC supply voltage range (V_{CCA}) ..... -0.3 to +3.0 V dc
Input voltage range (V_I) ..... -0.5 to +5.5 V dc
Input voltage(V_I) for bi-directional I/Os when using 3.3V PCI ..... -0.5 to (+V_{CCI} +0.5) V dc
Output voltage range (V_O) ..... -0.5 to (+V_{CCI} +0.5) V dc
Storage temperature range (V_{STG}) ..... -65 °C to +150 °C
Lead temperature (soldering, 10 seconds) ..... 300 °C
Thermal resistance, junction-to-case (Θ_{JC} for Case X and Y) ..... 2.0 °C/W
Maximum junction temperature (T_J) ..... 150 °C

1.4 Recommended operating conditions.

3.3V power supply voltage range ..... 3.0 to 3.6 V dc (±10% V_{CCI})
5.0V power supply voltage range ..... 4.5 to 5.5 V dc (±10% V_{CCI})
2.5V power supply voltage range ..... 2.25 to 2.75 V dc (±10% V_{CCA})
Case operating temperature range (T_C) ..... -55 °C to +125 °C
Input transition time T_R and T_F ..... 10 ns 5/

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012)..... 100 percent 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

5/ If T_R and T_F exceeds the limit of 10 ns, the device manufacturer cannot guarantee device functionality.

6/ 100 percent test coverage of blank programmable logic devices.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s).

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 90 percent of the total number of logic modules shall be utilized or at least 25 percent of the total logic modules shall be utilized for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Switching test circuit and waveforms. The switching test circuit and waveforms diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Binning program performed prior to burn-in.

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

d. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

e. Additional screening for devices 03, 04, 07, and 08 shall include:

(1) Internal visual, TM 2010 condition A

(2) 100% x-ray (top view only)

(3) 100% PIND (PIND is included for all devices (01 through 08))

(4) Serialization (Serialization is included for all devices (01 through 08))

(5) Static Burn-in, delta, read and record, PDA (3% functional)

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency equal or less than 1 MHz. Sample size is on a minimum of three devices with no failures on a minimum of five worst case pins from each device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on a minimum of three devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

e. Programmed device (see 3.2.3.2) - For device class M, subgroups 7, 8A, and 8B tests shall consist of verifying the functionality of the device. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, method 5012.

f. Unprogrammed devices shall be tested for programmability and dc and ac performance compliance to the requirements of group A, subgroups 1 and 7 (Note: The following steps are done prior to burn-in).

(1) Programming requirements shall be based on either wafer lot or assembly lot. An assembly lot is comprised of one or more wafers from the wafer lot. Sample size series shall be 8 devices with no programming failures. The occurrence of one programming failure will allow for an additional 5 samples to be tested with no additional programming failures allowed 13 (1). The occurrence of a second programming failure will allow for an additional 5 samples to be tested with no additional programming failures allowed 18(2). The occurrence of more than 3 programming failures during this process allows the manufacture to resubmit to a tightened sample size series of 48(3) or 85(7).

(2) Retesting of devices due to failure shall be in accordance with the manufacture's Quality Control Monitor (QCMON) for the purpose of determining the failure as True or False as defined in the QCMON.

(3) All units that have passed programming shall be tested for functionality. The occurrence of one DC failure at functional testing, shall require the manufacture to perform 100% electrical testing of the assembly or wafer lot followed by a functional test using a sample size series of 45(minimum) programmed devices with no failures. The assembly or wafer lot shall be rejected if there are functional failures or more than one DC failure.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ± 5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

TABLE I. Electrical performance characteristics. 1/ 2/

Operation with V_{CCI} = 3.3V or V_{CCI} = 5.0V (for 3.3V LVTTL and 5V TTL I/O Operations)

Test	Symbol	Conditions 3/ 2.25 V ≤ V_{CCA} ≤ 2.75 V 3.0 V ≤ V_{CCI} ≤ 3.6 V or 4.5 V ≤ V_{CCI} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CCI} = Min., V_I = V_{IH} or V_{IL} I_{OH} = -1 mA	1,2,3	All	0.9 V_{CCI}		V
		V_{CCI} = Min., V_I = V_{IH} or V_{IL} I_{OH} = -8 mA			2.4		
Low level output voltage	V_{OL}	V_{CCI} = Min., V_I = V_{IH} or V_{IL} I_{OL} = 1 mA	1,2,3	All		0.1 V_{CCI}	V
		V_{CCI} = Min., V_I = V_{IH} or V_{IL} I_{OH} = 12 mA				0.40	
Low level input voltage	V_{IL}		1,2,3	All		0.8	V
High level input voltage	V_{IH}		1,2,3	All	2.0		V
Input leakage current	I_{IL}	V_{IN} = V_{CCI} or GND	1,2,3	01,02, 03,04	-20	20	µA
		V_{IN} = V_{CCI} or GND and 4.5 V ≤ V_{CCI} ≤ 5.25 V		05,06, 07,08	-20	20	µA
		V_{IN} = V_{CCI} or GND and 5.25 V < V_{CCI} ≤ 5.5 V		05,06, 07,08	-70	70	µA
3-state output leakage current	I_{OZ}	V_{OUT} = V_{CCI} or GND	1,2,3	01,02, 03,04	-20	20	µA
		V_{IN} = V_{CCI} or GND and 4.5 V ≤ V_{CCI} ≤ 5.25 V		05,06, 07,08	-20	20	µA
		V_{IN} = V_{CCI} or GND and 5.25 V < V_{CCI} ≤ 5.5 V		05,06, 07,08	-70	70	µA
I/O terminal capacitance	$C_{I/O}$ & C_{CLK}	See 4.4.1c f ≤ 1.0 MHz, V_{OUT} ≈ 0 V	4	All		20	pF
Standby supply current	I_{CC} 4/		1,2,3	All		25	mA
Functional tests	FT 5/	See 4.4.1e	7,8A,8B	All			
Binning circuit delay	t_{PBLH}, t_{PBHL} 6/ 7/	See figure 3, V_{IH} = 3.0 V, V_{IL} = 0 V, V_{OUT} = 1.5 V, V_{CCA} = 2.5 V, V_{CCI} = 3.3 V	9	01, 03 05,07		97	ns
				02, 04 06,08		82	

See notes at end of Table I.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Operation with V_{CCI} = 5.0V (for 5V CMOS I/O Operations)

Test	Symbol	Conditions 3/ 2.25 V ≤ V_{CCA} ≤ 2.75 V 4.5 V ≤ V_{CCI} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CCI} = Min., V_I = V_{CCI} or GND I_{OH} = -20µA	1,2,3	All	V_{CCI} - 0.1		V
Low level output voltage	V_{OL}	V_{CCI} = Min., V_I = V_{CCI} or GND I_{OL} = +20 µA	1,2,3	All		0.1	V
Low level input voltage	V_{IL}	V_{OUT} ≤ V_{VOL}(Max)	1,2,3	All		0.3 V_{CCI}	V
High level input voltage	V_{IH}	V_{OUT} ≥ V_{VOH}(Max)	1,2,3	All	0.7 V_{CCI}		V
3-state output leakage current	I_{OZ}	V_{OUT} = V_{CCI} or GND	1,2,3	01,02, 03,04	-20	20	µA
		V_{IN} = V_{CCI} or GND and 4.5 V ≤ V_{CCI} ≤ 5.25 V		05,06, 07,08	-20	20	µA
		V_{IN} = V_{CCI} or GND and 5.25 V < V_{CCI} ≤ 5.5 V		05,06, 07,08	-70	70	µA
I/O terminal capacitance	$C_{I/O}$ & C_{CLK}	See 4.4.1c f ≤ 1.0 MHz, V_{OUT} ≈ 0 V	4	All		20	pF
Standby supply current	I_{CC} 4/		1,2,3	All		25	mA
Functional tests	FT 5/	See 4.4.1e	7,8A,8B	All			

See notes at end of Table I.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Operation with V_{CCI} = 5.0V (for 5.0V PCI I/O Operations, 8/)

Test	Symbol	Conditions 3/ 2.25 V ≤ V_{CCA} ≤ 2.75 V 4.5 V ≤ V_{CCI} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}		1,2,3	All	2.0	V_{CCI} +0.5	V
Low level input voltage	V_{IL}		1,2,3	All	-0.5	0.8	V
Input high leakage current	I_{IH}	V_{IN} = 2.75 V	1,2,3	All		70	µA
Input low leakage current	I_{IL}	V_{IN} = 0.5 V	1,2,3	All		-70	µA
High level output voltage	V_{OH}	I_{OUT} = -2mA	1,2,3	All	2.4		V
Low level output voltage	V_{OL} 9/	I_{OUT} = 3mA, 6mA	1,2,3	All		0.55	V
Input pin capacitance	C_{IN} 10/		4	All		10	pF
Clock pin capacitance	C_{CLK} 10/		4	All	5	12	pF

See notes at the end of Table I.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Operation with V_{CCI} = 3.3V (for 3.3V PCI I/O Operations, 8/)

Test	Symbol	Conditions 3/ 2.25 V ≤ V_{CCA} ≤ 2.75 V 3.0 V ≤ V_{CCI} ≤ 3.6 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}		1,2,3	All	0.5 V_{CCI}	V_{CCI} +0.5	V
Low level input voltage	V_{IL}		1,2,3	All	-0.5	0.3 V_{CCI}	V
Input pull-up voltage	I_{IPU} 11/		1,2,3	All	0.7 V_{CCI}		V
Input leakage current	I_{IH} / I_{IL}	0 ≤ V_{IN} ≤ V_{CCI}	1,2,3	All	-20	20	µA
High level output voltage	V_{OH}	I_{OUT} = -500 µA	1,2,3	All	0.9 V_{CCI}		V
Low level output voltage	V_{OL}	I_{OUT} = 1500 µA	1,2,3	All		0.1 V_{CCI}	V
Input pin capacitance	C_{IN} 10/		4	All		10	pF
Clock pin capacitance	C_{CLK} 10/		4	All	5	12	pF

1/ AC/Timing parameters (subgroup 9, 10, 11) are not directly tested but fully characterized (see note 2/), which are published on device manufacturer's data sheet and implemented in manufacturer's software (see 6.7 and Table IIA note 8/ herein).

2/ Characterization data is taken at initial device introduction and repeated after any design or process changes that may affect the related parameters. Devices are first 100 percent functionally tested, then benchmark design/timing patterns are programmed into the devices and then characterized to determine the compliance of the parameters.

3/ All tests shall be performed under the worst-case condition unless otherwise specified.

4/ Standby I_{CC} is the total standby current of I_{CCA} and I_{CCI}.

5/ Devices are functionally tested using a serial scan test method. Data is shifted into the TDI pin and the TCK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the PRA, PRB, or TDO pins.

6/ Binning circuit delay is defined as the input-to-output delay of a special path called the "binning circuit". The binning circuit consists of one input buffer plus a fixed number of combinatorial logic modules plus on output buffer. These modules are configured as non-inverting buffers and are connected through programmed antifuses with typical capacitive loading.

7/ Binning circuit parameters are tested with typical conditions as listed in this table at room temperature only. Measurement of binning circuit propagation delay may be used to distinguish standard and –1 speed devices. However, the performance of user designs are mainly affected by variations introduced in individual designs. Therefore, measurement difference in binning circuit speed shall not be used for picking faster devices from devices of the same speed grade.

8/ This device is electrically compliant with the PCI Local Bus Specification Rev. 2.2.

9/ Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.

TABLE I. Electrical performance characteristics Continued. 1/ 2/

10/ Absolute maximum pin capacitance for a PCI input is 10 pF. Exceptions will be for clock pins including CLK A/B, and HCLK.

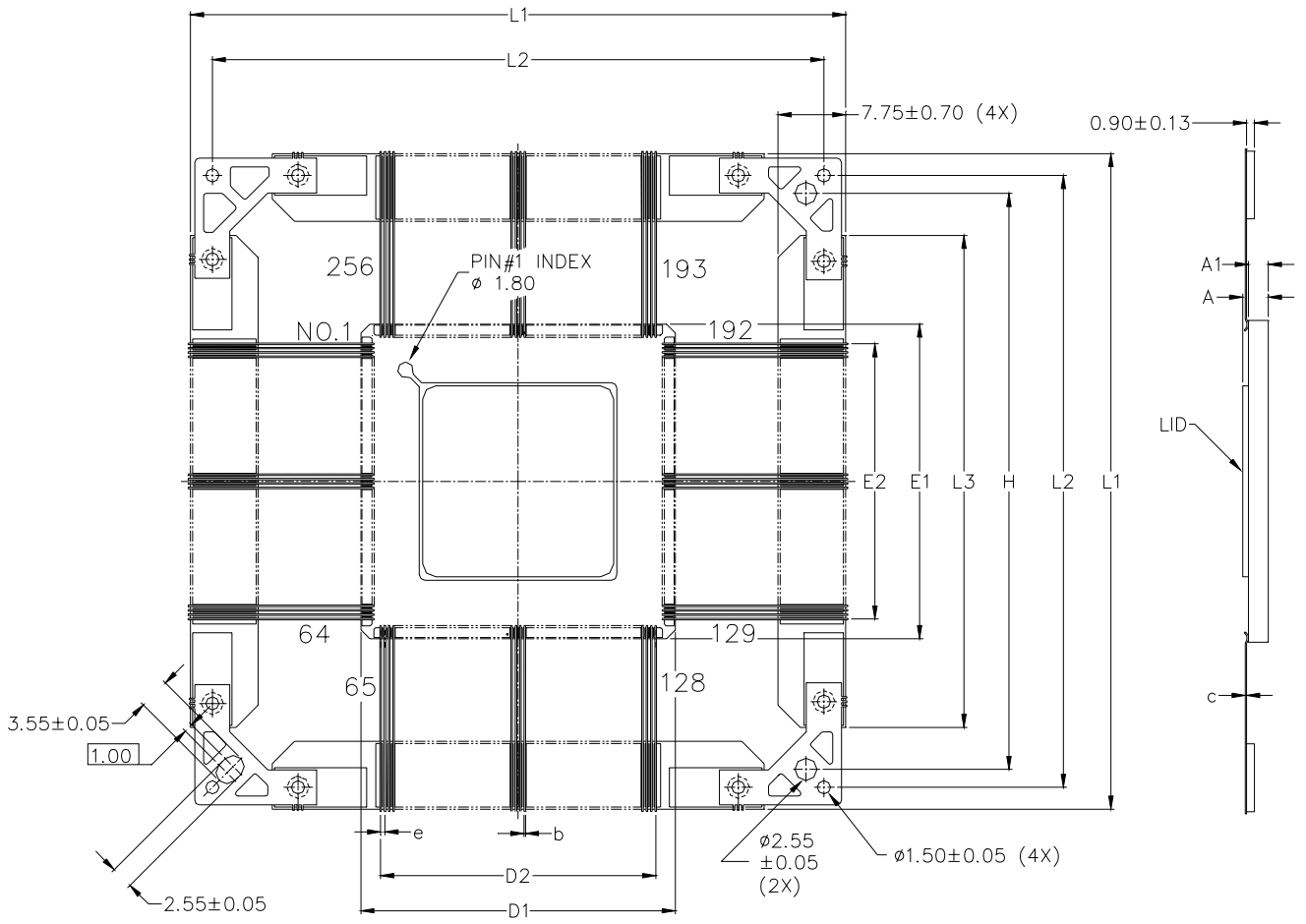
11/ This parameter (I_{IPU}) is not directly tested but fully characterized (see 2/). It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.
8/ Subgroups 9,10, and 11 switching parameters, if not provided in table I, shall be designated by device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be maintained under document revision level control, and shall be made available to the acquiring or preparing activity upon request.

Case Outline X



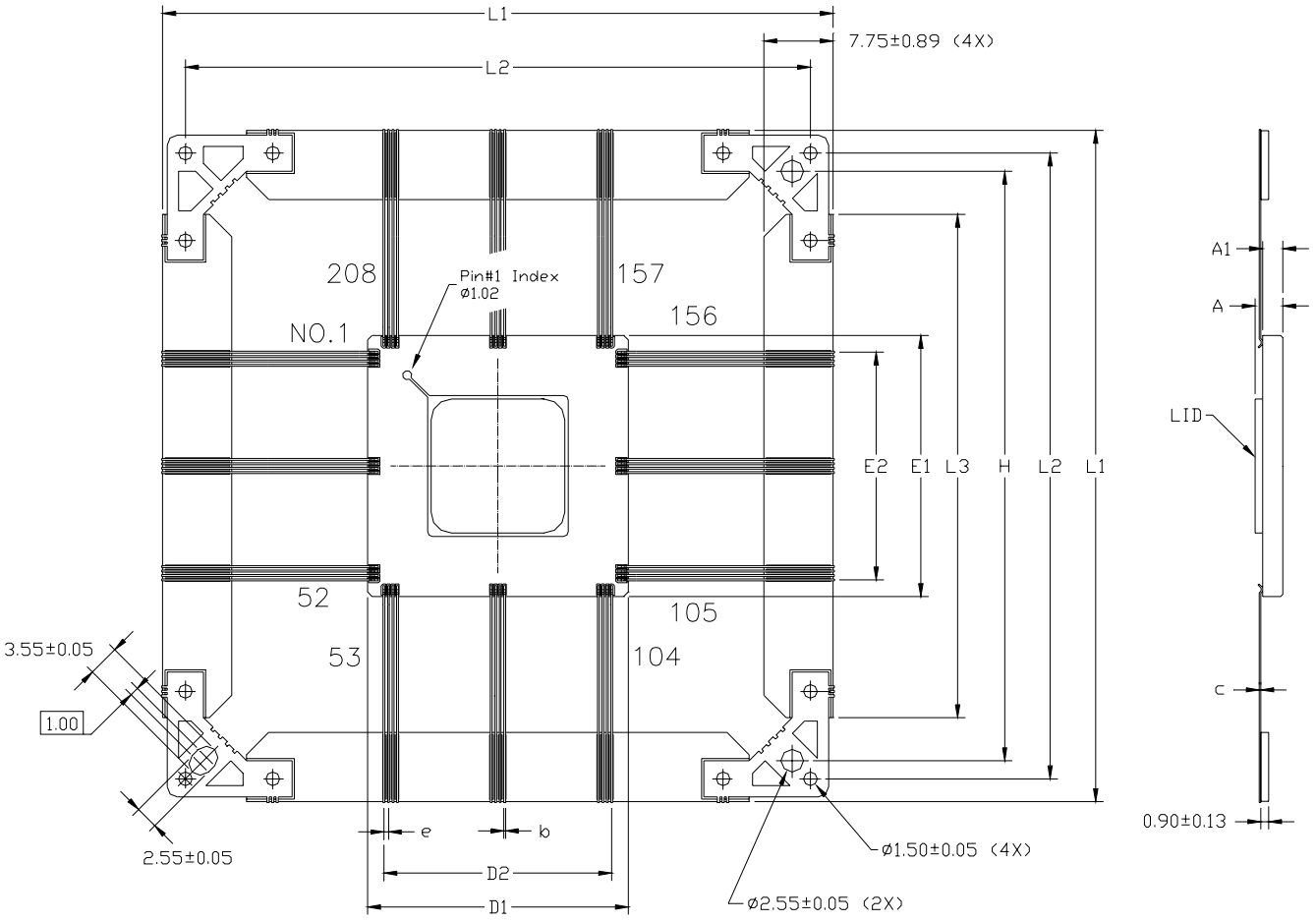
NOTES:

1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 µm) minimum thickness over 80 to 350 microinches (2.0 to 8.9 µm) thickness of nickel
2. Seal ring area is connected to GND.
3. Die attach pad is connected to GND.
4. 15 gm weight is measured after tie-bar removed.
5. Tie-bar dimensions are for reference only.

Symbol	Dimension (unit : mm)		
	Min.	Norm.	Max.
A	2.50	2.86	3.22
A1	2.04	2.29	2.54
b	0.18	0.20	0.23
c	0.10	0.15	0.18
D1/E1	35.64	36.00	36.36
D2/E2	31.50 BSC		
e	0.50 BSC		
L1	74.60	75.00	75.40
L2	70.00 BSC		
L3	56.30 BSC		
H	65.90 BSC		
Weight	15 gm (typical)		

FIGURE 1. Case outline.

Case Outline Y



Symbol	Dimension (unit : mm)		
	Min.	Norm.	Max.
A	2.50	2.86	3.22
A1	2.04	2.29	2.54
b	0.18	0.20	0.23
c	0.10	0.15	0.20
D1/E1	28.96	29.21	29.46
D2/E2	25.50 BSC		
e	0.50 BSC		
L1	74.60	75.00	75.40
L2	70.00 BSC		
L3	56.30 BSC		
H	65.90 BSC		
Weight	8.6 gm (typical)		

NOTES:

1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 µm) minimum thickness over 80 to 350 microinches (2.0 to 8.9 µm) thickness of nickel.
2. Seal ring area is connected to GND.
3. Die attach pad is connected to GND.
4. 8.6 gm weight is measured after tie-bar removed.
5. Tie-bar dimensions are for reference only.

FIGURE 1. Case outline. – Continued.

Case Outline X

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	44	I/O	87	I/O
2	TDI, I/O	45	I/O	88	I/O
3	I/O	46	VCCA	89	I/O
4	I/O	47	I/O	90	PRB, I/O
5	I/O	48	I/O	91	GND
6	I/O	49	I/O	92	VCCI
7	I/O	50	I/O	93	GND
8	I/O	51	I/O	94	VCCA
9	I/O	52	I/O	95	I/O
10	I/O	53	I/O	96	HCLK
11	TMS	54	I/O	97	I/O
12	I/O	55	I/O	98	I/O
13	I/O	56	I/O	99	I/O
14	I/O	57	I/O	100	I/O
15	I/O	58	I/O	101	I/O
16	I/O	59	GND	102	I/O
17	I/O	60	I/O	103	I/O
18	I/O	61	I/O	104	I/O
19	I/O	62	I/O	105	I/O
20	I/O	63	I/O	106	I/O
21	I/O	64	I/O	107	I/O
22	I/O	65	I/O	108	I/O
23	I/O	66	I/O	109	I/O
24	I/O	67	I/O	110	GND
25	I/O	68	I/O	111	I/O
26	I/O	69	I/O	112	I/O
27	I/O	70	I/O	113	I/O
28	VCCI	71	I/O	114	I/O
29	GND	72	I/O	115	I/O
30	VCCA	73	I/O	116	I/O
31	GND	74	I/O	117	I/O
32	I/O	75	I/O	118	I/O
33	I/O	76	I/O	119	I/O
34	TRST	77	I/O	120	I/O
35	I/O	78	I/O	121	I/O
36	I/O	79	I/O	122	I/O
37	I/O	80	I/O	123	I/O
38	I/O	81	I/O	124	I/O
39	I/O	82	I/O	125	I/O
40	I/O	83	I/O	126	TDO, I/O
41	I/O	84	I/O	127	I/O
42	I/O	85	I/O	128	GND
43	I/O	86	I/O	129	I/O

FIGURE 2. Terminal connections.

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
130	I/O	173	I/O	216	I/O
131	I/O	174	VCCA	217	I/O
132	I/O	175	GND	218	I/O
133	I/O	176	GND	219	CLKA
134	I/O	177	I/O	220	CLKB
135	I/O	178	I/O	221	VCCI
136	I/O	179	I/O	222	GND
137	I/O	180	I/O	223	NC
138	I/O	181	I/O	224	GND
139	I/O	182	I/O	225	PRA, I/O
140	I/O	183	I/O	226	I/O
141	VCCA	184	I/O	227	I/O
142	I/O	185	I/O	228	I/O
143	I/O	186	I/O	229	I/O
144	I/O	187	I/O	230	I/O
145	I/O	188	I/O	231	I/O
146	I/O	189	GND	232	I/O
147	I/O	190	I/O	233	I/O
148	I/O	191	I/O	234	I/O
149	I/O	192	I/O	235	I/O
150	I/O	193	I/O	236	I/O
151	I/O	194	I/O	237	I/O
152	I/O	195	I/O	238	I/O
153	I/O	196	I/O	239	I/O
154	I/O	197	I/O	240	GND
155	I/O	198	I/O	241	I/O
156	I/O	199	I/O	242	I/O
157	I/O	200	I/O	243	I/O
158	GND	201	I/O	244	I/O
159	NC	202	I/O	245	I/O
160	GND	203	I/O	246	I/O
161	VCCI	204	I/O	247	I/O
162	I/O	205	I/O	248	I/O
163	I/O	206	I/O	249	I/O
164	I/O	207	I/O	250	I/O
165	I/O	208	I/O	251	I/O
166	I/O	209	I/O	252	I/O
167	I/O	210	I/O	253	I/O
168	I/O	211	I/O	254	I/O
169	I/O	212	I/O	255	I/O
170	I/O	213	I/O	256	TCK, I/O
171	I/O	214	I/O		
172	I/O	215	I/O		

FIGURE 2. Terminal connections. – Continued.

Case Outline Y

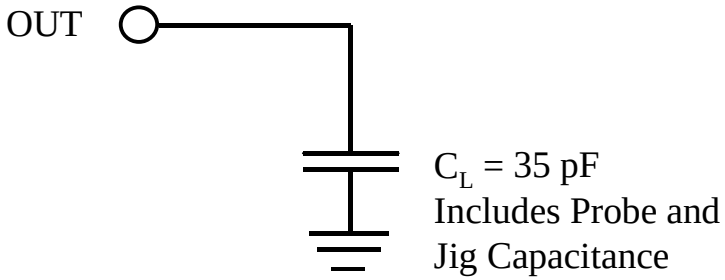
Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	36	I/O	71	I/O
2	TDI, I/O	37	I/O	72	I/O
3	I/O	38	I/O	73	I/O
4	I/O	39	I/O	74	I/O
5	I/O	40	VCCI	75	I/O
6	I/O	41	VCCA	76	PRB, I/O
7	I/O	42	I/O	77	GND
8	I/O	43	I/O	78	VCCA
9	I/O	44	I/O	79	GND
10	I/O	45	I/O	80	NC
11	TMS	46	I/O	81	I/O
12	VCCI	47	I/O	82	HCLK
13	I/O	48	I/O	83	I/O
14	I/O	49	I/O	84	I/O
15	I/O	50	I/O	85	I/O
16	I/O	51	I/O	86	I/O
17	I/O	52	GND	87	I/O
18	I/O	53	I/O	88	I/O
19	I/O	54	I/O	89	I/O
20	I/O	55	I/O	90	I/O
21	I/O	56	I/O	91	I/O
22	I/O	57	I/O	92	I/O
23	I/O	58	I/O	93	I/O
24	I/O	59	I/O	94	I/O
25	NC	60	VCCI	95	I/O
26	GND	61	I/O	96	I/O
27	VCCA	62	I/O	97	I/O
28	GND	63	I/O	98	VCCI
29	I/O	64	I/O	99	I/O
30	TRST	65	NC	100	I/O
31	I/O	66	I/O	101	I/O
32	I/O	67	I/O	102	I/O
33	I/O	68	I/O	103	TDO, I/O
34	I/O	69	I/O	104	I/O
35	I/O	70	I/O	105	GND

FIGURE 2. Terminal connections. – Continued.

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
106	I/O	141	I/O	176	I/O
107	I/O	142	I/O	177	I/O
108	I/O	143	I/O	178	I/O
109	I/O	144	I/O	179	I/O
110	I/O	145	VCCA	180	CLKA
111	I/O	146	GND	181	CLKB
112	I/O	147	I/O	182	NC
113	I/O	148	VCCI	183	GND
114	VCCA	149	I/O	184	VCCA
115	VCCI	150	I/O	185	GND
116	I/O	151	I/O	186	PRA, I/O
117	I/O	152	I/O	187	I/O
118	I/O	153	I/O	188	I/O
119	I/O	154	I/O	189	I/O
120	I/O	155	I/O	190	I/O
121	I/O	156	I/O	191	I/O
122	I/O	157	GND	192	I/O
123	I/O	158	I/O	193	I/O
124	I/O	159	I/O	194	I/O
125	I/O	160	I/O	195	I/O
126	I/O	161	I/O	196	I/O
127	I/O	162	I/O	197	I/O
128	I/O	163	I/O	198	I/O
129	GND	164	VCCI	199	I/O
130	VCCA	165	I/O	200	I/O
131	GND	166	I/O	201	VCCI
132	NC	167	I/O	202	I/O
133	I/O	168	I/O	203	I/O
134	I/O	169	I/O	204	I/O
135	I/O	170	I/O	205	I/O
136	I/O	171	I/O	206	I/O
137	I/O	172	I/O	207	I/O
138	I/O	173	I/O	208	TCK, I/O
139	I/O	174	I/O		
140	I/O	175	I/O		

FIGURE 2. Terminal connections. – Continued.

TEST LOAD



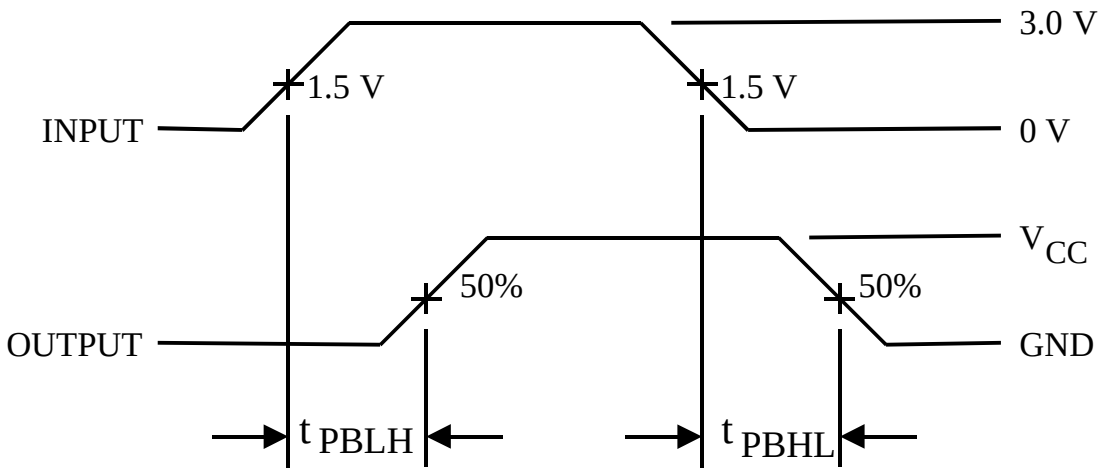


FIGURE 3. Switching test circuit and waveforms. 1/

1/ Loading for 3.3 V PCI is 10 pF and 5 V PCI is 50 pF.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types	
	01, 02, 03, 04	05, 06, 07, 08
I_{CC}	± 1 mA of specified value in table I	± 5 mA of specified value in table I
I_{OZ}	± 2 µA of specified value in table I	± 5 µA of specified value in table I
t_{PBLH}, t_{PBHL}	± 10 ns	± 10 ns

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Design characteristics. The complexity of the devices covered by this document, will require the user/designer to be familiar with additional design characteristics of the device. Contact the manufacturer for design and functional support. Updated versions of device manufacturer's software, device data sheet, IBIS models, and application notes may be obtained directly from device manufacturer's website (http://www.actel.com).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 27 August 2004

Approved sources of supply for SMD 5962-01508 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0150801QXC	0J4Z0	RT54SX32S-CQ256B
5962-0150801QYC	0J4Z0	RT54SX32S -CQ208B
5962-0150802QXC	0J4Z0	RT54SX32S -1CQ256B
5962-0150802QYC	0J4Z0	RT54SX32S -1CQ208B
5962-0150803QXC	0J4Z0	RT54SX32S -CQ256E
5962-0150803QYC	0J4Z0	RT54SX32S -CQ208E
5962-0150804QXC	0J4Z0	RT54SX32S -1CQ256E
5962-0150804QYC	0J4Z0	RT54SX32S -1CQ208E
5962-0150805QXC	0J4Z0	RTSX32SU-CQ256B
5962-0150805QYC	0J4Z0	RTSX32SU-CQ208B
5962-0150806QXC	0J4Z0	RTSX32SU-1CQ256B
5962-0150806QYC	0J4Z0	RTSX32SU-1CQ208B
5962-0150807QXC	0J4Z0	RTSX32SU-CQ256E
5962-0150807QYC	0J4Z0	RTSX32SU-CQ208E
5962-0150808QXC	0J4Z0	RTSX32SU-1CQ256E
5962-0150808QYC	0J4Z0	RTSX32SU-1CQ208E

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0J4Z0	Actel Corporation 2061 Stierlin Court. Mountain View, CA 94043